

ABSTRACT

DESIGN AND IMPLEMENTATION OF SPI USING VHDL

Objective of the project:

1. Study of SPI
2. Behavioral/RTL modeling of Design blocks
3. Design of stimulus modules to test the functionality of Design.
4. Synthesize design to extract Gate level net list.
5. Perform the post Synthesis (Logical) Simulation of the design

Description:

The target domain for this project is networking. We choose serial data transfer over parallel data transfer because parallel data transfer take more number of Wires, which increases hardware. Its main use is to replace parallel interfaces so, we don't have to route parallel buses around a PCB. For example we can buy an SPI 12bit ADC and instead of 12 parallel wires to read the data we need 4 spi connection. actually we may need three as we may not need to send the data to the device.

With the spi interface we can communicate with a device transmitting and receiving 8 bits of data at the same time and it is suited to high speed streaming data transfers.

SPI is a much simple protocol and because of this we can operate speeds greater than 10mhz(compared with 3,4MHZ maximum for I2c).The best feature of spi is that we can do full duplex data transfers(data in both directions at the same time) which we an not with I2c and we can do it fast.

This Design coding, Simulation, Logic Synthesis and Implemented will be done using various EDA tools

SPI CONTROL BLOCK DIAGRAM

