

ABSTRACT

DESIGN AND IMPLEMENTATION OF DIFFERENT ADDERS USING VHDL

Objective of the project:

1. Study of Look Different Adders.
2. Behavioral/RTL modeling of Design blocks.
3. Design of stimulus modules to test the functionality of Design.
4. Synthesize design to extract Gate level net list.
5. Perform the post Synthesis (Logical) Simulation of the design

Description:

Carry look-ahead adder:

A carry look-ahead adder improves speed by reducing the amount of time required to determine carry bits. It can be contrasted with the simpler, but usually slower. This adder is a practical design with reduced delay at the price of more complex hardware. The carry look-ahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits.

Ripple Carry Adder:

Ripple-carry adders the simplest and most compact parallel adders require as little as four cells per bit, and one layout has a carry delay of only one cell per bit. These are slower. The delay of a carry look ahead adder grows logarithmically with the size of the adder, while a ripple carry adder's delay grows linearly.

This Design coding, Simulation, Logic Synthesis and Implemented will be done using various EDA tools.