

ABSTRACT

DESIGN AND IMPLEMENTATION OF ARITHMETIC LOGIC UNIT

Objective of the project:

1. Study of ARITHMETIC LOGIC UNIT
2. Behavioral/RTL modeling of Design blocks
3. Design of stimulus modules to test the functionality of Design.
4. Synthesize design to extract Gate level net list.
5. Perform the post Synthesis (Logical) Simulation of the design

Description:

Arithmetic Logic Unit (ALU) is a digital circuit that performs arithmetic and logical operations. The ALU is a fundamental building block of the central processing unit (CPU) of a computer, and even the simplest microprocessors contain one for purposes such as maintaining timers.

An ALU must process numbers using the same format as the rest of the digital circuit. ALUs for each one of these numeric systems had different designs, and that influenced the current preference for two's complement, as this is the representation that makes it easier for the ALUs to calculate additions and subtractions.

Most of a processor's operations are performed by one or more ALUs. An ALU loads data from input registers, an external Control Unit then tells the ALU what operation to perform on that data, and then the ALU stores its result into an output register. Other mechanisms move data between these registers and memory.

This Design coding, Simulation, Logic Synthesis and Implemented will be done using various EDA tools.